DETAILED ACTION

This is a non-final action in response to the remarks dated 02/09/2010.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claim 1 is rejected under 35 U.S.C. 102(e) as anticipated by 2006/0035164 (Schaper).

Schaper provides a template (figure 13) formed from a layered structure (layers 630, 620, 610, 1302) comprising a single-phase polymer layer (610) positioned on the substrate (1302); and a semiconductor or metal layer positioned on the polymer layer

(630, 620 combination); wherein the polymer layer comprises a textured surface (612). The limitations "the texturing being caused by induction of stress in the polymer layer with the semiconductor or metal layer present" and "baking of the polymer layer at a temperature below the glass transition temperature of the polymer" are process limitations included in a product claim. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985), MPEP 2113. Since the products are the same, the process limitations are not given patentable weight.

3. Claims 1, 4, 5, 7, and 8 are rejected under 35 U.S.C. 102(e) as anticipated by 2006/0035164 (Schaper).

Schaper provides a template (figure 13) formed from a layered structure (layers 630, 620, 610, 1302) comprising a single-phase polymer layer (610) positioned on the substrate (630/620 combination); and a semiconductor or metal layer positioned on the polymer layer (1302); wherein the polymer layer comprises a textured surface (612). The limitations "the texturing being caused by induction of stress in the polymer layer with the semiconductor or metal layer present" and "baking of the polymer layer at a temperature below the glass transition temperature of the polymer" are process limitations included in a product claim. "[E]ven though product-by-process claims are

limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985), MPEP 2113. Since the products are the same, the process limitations are not given patentable weight.

Claim 4:

Schaper teaches that other materials are suitable for use in the formation of the substrate such as Ge [0067].

Claim 5:

Schaper uses silicon as a substrate material [0067].

Claim 7:

Schaper teaches the formation of a pattern layer having the dimensions of between 20nm to 100 nm and also a method for altering the sizes of such a layer [0081]. Schaper teaches the use of a substrate comprising silicon [0053].

Claim 8:

Schaper teaches that the sputtered on layer has a thickness of about 10nm [0058].

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 2006/0035164 (Schaper).

Claim 6:

Schaper does not teach that the pattern comprises parallel groves. Schaper does teach a patterning method which is capable of producing such structures [0063], [0065]. It would have been obvious to one having ordinary skill in the art at the time of the invention to shape the pattern in the form of parallel lines motivated by choice of design.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 2006/0035164 (Schaper) in view of US 2002/0042027 (Chou).

Schaper teaches the limitations of applicant's claims previously presented but does not teach the use of PMMA. Chou teaches the use of PMMA [0035] also in a process forming a template (combination of elements 31 and 33). Chou also teaches a method of deforming the polymer layer of PMMA, LISA [0012]. The PMMA polymer would perform as intended in the invention of Schaper. It would have been obvious to one having ordinary skill in the art at the time of the invention motivated by a desire to shape the polymer layer by the LISA process used in Chou.

6. Claims 1, 3-8, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 2002/0042027 (Chou) in view of US 2006/0035164 (Schaper).

Claim 1:

Chou provides a template (combination of elements 31 and 33) formed from a layered structure (layers 31 and 33), comprising a substrate (31) and a single-phase polymer layer positioned on the substrate (33). Chou teaches the polymer layer comprises a textured surface (49), the texturing being caused by induction of stress in the polymer (LISA, [0012]) layer with the semiconductor (31 is a semiconductor [0035]) or metal

layer present, after baking of the polymer layer at a temperature below the glass transition temperature [0035] of the polymer.

Chou does not teach the use of an additional layer such that there is a substrate layer separate from the semiconductor layer with a polymer layer in between. Schaper provides a template (figure 13) formed from a layered structure (layers 630, 620, 610, 1302) comprising a single-phase polymer layer (610) positioned on the substrate (630/620 combination); and a semiconductor or metal layer positioned on the polymer layer (1302); wherein the polymer layer comprises a textured surface (612).

The claim requires a product: a template. Schaper teaches that the metal layer added improves the durability of the template [0011]. It would have been obvious to one having ordinary skill in the art at the time of the invention to use the metal coating of Schaper in the invention of Chou motivated by a desire to protect the template. The process limitation "induction of stress in the polymer layer with the semiconductor or metal layer present" is a process limitation embedded in a product claim and is therefore not given patentable weight.

Claim 3:

Chou uses PMMA.

Claim 4:

Schaper teaches that other materials are suitable for use in the formation of the substrate such as Ge [0067].

Claim 5:

Chou uses silicon as a substrate material.

Claim 6:

Such can be seen in Chou figures 14.

Claim 7:

Chou teaches the dimensions required by the claims [0013].

Claim 8:

Schaper teaches that the sputtered on layer has a thickness of about 10nm [0058].

Claim 27:

Chou teaches stabilization by annealing after the induction of stress [0035].

Response to Arguments

1. Applicant's arguments filed 9 FEB 2010 have been fully considered but they are not persuasive.

2. Applicant's argument that the substrate 31 is not the claimed "semiconductor layer" because claim 1 recites that the "semiconductor or metal layer" is "positioned on the polymer layer" has been considered but it is not persuasive. Substrate 31 is a semiconductor and it is in contact with the polymer layer. The examiner considers layers that are in contact with each other to be "on" each other. This is because such prepositions as "on, above, upon, underneath..." etc are relational. When the product is turned upside down, "underneath" becomes "on top of". The product does not change. If a piece of toast, buttered on the top, is dropped onto the floor such that the buttered side lands on the bottom, the toast is still the same. Thus the examiner considers "on and underneath" to be the same; they do not change the structure of the claimed product.

3. Applicant's argument that the silicon wafer substrate in Chou is not positioned on the polymer layer has been considered but it is not persuasive. Applicant argues that the substrate is under the polymer layer. If that is the case, the substrate is in contact with the polymer layer. Simply turning the product upside down does not change the structure of or method of making the product at all.

Applicant's argument that positioning the PMMA on the semiconductor does not satisfy the requirement of "a semiconductor or metal layer positioned on the polymer layer" has been considered. This is not found to be persuasive because such amounts to turning the product upside down.

4. Applicant's argument that the substrate and the semiconductor layer are not the same has been considered but it is not persuasive. Even if, *arguendo*, there must be three layers the new ground of rejection provides three layers. Thus such an argument is moot.

5. Applicant's argument that the combination of Chou and Schaper does not teach texturing being caused by the induction of stress with the semiconductor or metal layer present has been considered but it is not persuasive. The substrate is present in each of figures 1A-D. The formation of the pattern is shown in these figures. In each of the figures, the substrate is present. But, the substrate in this case is a semiconductor. Schaper provides an additional layer; a metal layer. The claim requires either a semiconductor layer or metal layer be present at the time of the stress induction. In this case, the semiconductor layer is present and the metal layer is sputtered on afterward. This is shown in Chou, figures 1A-D.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID N. BROWN II whose telephone number is (571)270-5497. The examiner can normally be reached on Monday-Thursday 7:30a-5:00p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph Del Sole can be reached on (571)-272-1130. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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